



**EV371300616**

Inventor: **Yoshiki Hishiro**  
Title: **Methods of Forming Semiconductor Constructions**  
Assignee: **Micron Technology, Inc.**  
Serial No.: **10/783,419**  
Filed: **February 19, 2004 [RCE Filed Herewith]**

**INFORMATION DISCLOSURE STATEMENT**

**PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98**

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, the Examiner's attention is directed to the reference listed on the attached Form PTO-1449. The attached Form PTO-1449 is submitted in compliance with 37 CFR §1.56. Pursuant to FEDERAL REGISTER, Vol. 69, No. 182, pg. 56542 (September 21, 2004), no copies of any cited U.S. patents or U.S. published applications are included herewith.

No admission is made regarding whether the submitted reference is prior art.

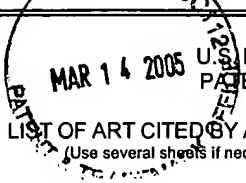
Citation of this patent is respectfully requested.

Respectfully submitted,

Date: 3/14/05

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Form PTO-1449				<b>EV371300616</b>		ATTY. DOCKET NO. MI22-2507		SERIAL NO. 10/783,419	
LIST OF ART CITED BY APPLICANT <small>(Use several sheets if necessary)</small>				APPLICANT: Yoshiki Hishiro				GROUP 2814	
				FILING DATE Feb. 19, 2004 [RCE filed herewith]					
<b>U.S. PATENT DOCUMENTS</b>									
*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA	6,121,133	09/00	Iyer et al.					
	AB								
	AC								
	AD								
	AE								
	AF								
	AG								
	AH								
	AI								
<b>FOREIGN PATENT DOCUMENTS</b>									
		Document Number	Date	Country	Class	Subclass	Translation		
							Yes	No	
	AJ								
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<b>OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)</b>									
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<small>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>									